G1069

ARRAY OF GATE DIELECTRIC STRUCTURES TO MEASURE GATE DIELECTRIC THICKNESS AND PARASITIC CAPACITANCE

ABSTRACT OF THE DISCLOSURE

Accurate determination of gate dielectric thickness is required to produce high-reliability and high-performance ultra-thin gate dielectric semiconductor devices. Large area gate dielectric capacitors with ultra-thin gate dielectric layers suffer from high gate leakage, which prevents the accurate measurement of gate dielectric thickness. Accurate measurement of gate dielectric thickness of smaller area gate dielectric capacitors is hindered by the relatively large parasitic capacitance of the smaller area capacitors. The formation of first and second dummy structures on a wafer allow the accurate determination of gate dielectric thickness. First and second dummy structures are formed that are substantially similar to the gate dielectric capacitors except that the first dummy structures are formed without the second electrode of the capacitor and the second dummy structures are formed without the first electrode of the capacitor structure. The capacitance, and therefore thickness, of the gate dielectric capacitor is determined by subtracting the parasitic capacitances measured at the first and second dummy structures.